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**PATENT APPLICATION**  
Volkmar Schroth

**Case** 4  
**Serial No.** 09/228,101 **Filed** 01/11/99  
**Examiner** Kevin C. Harper **Group Art Unit** 2664

**Title** Circuit For Transmitting Plesiochronous Signals In A SDH System

**ASSISTANT COMMISSIONER FOR PATENTS**  
WASHINGTON, D. C. 20231

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JUL 22 2002

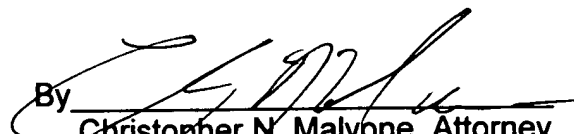
Technology Center 2600

**SIR:**

**ATTENTION: Patent Office Draftsperson**

Transmitted herewith are six (6) sheets of formal drawing(s) to be substituted for the informal drawing(s) initially filed in the above-identified application for patent.

Respectfully,  
Volkmar Schroth

By   
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Att:  
6 Sheets Formal drawings

Date: July 11, 2002

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D. C. 20231 on July 11, 2002.

  
Margaret Cardoso

1/6

FIG. 1

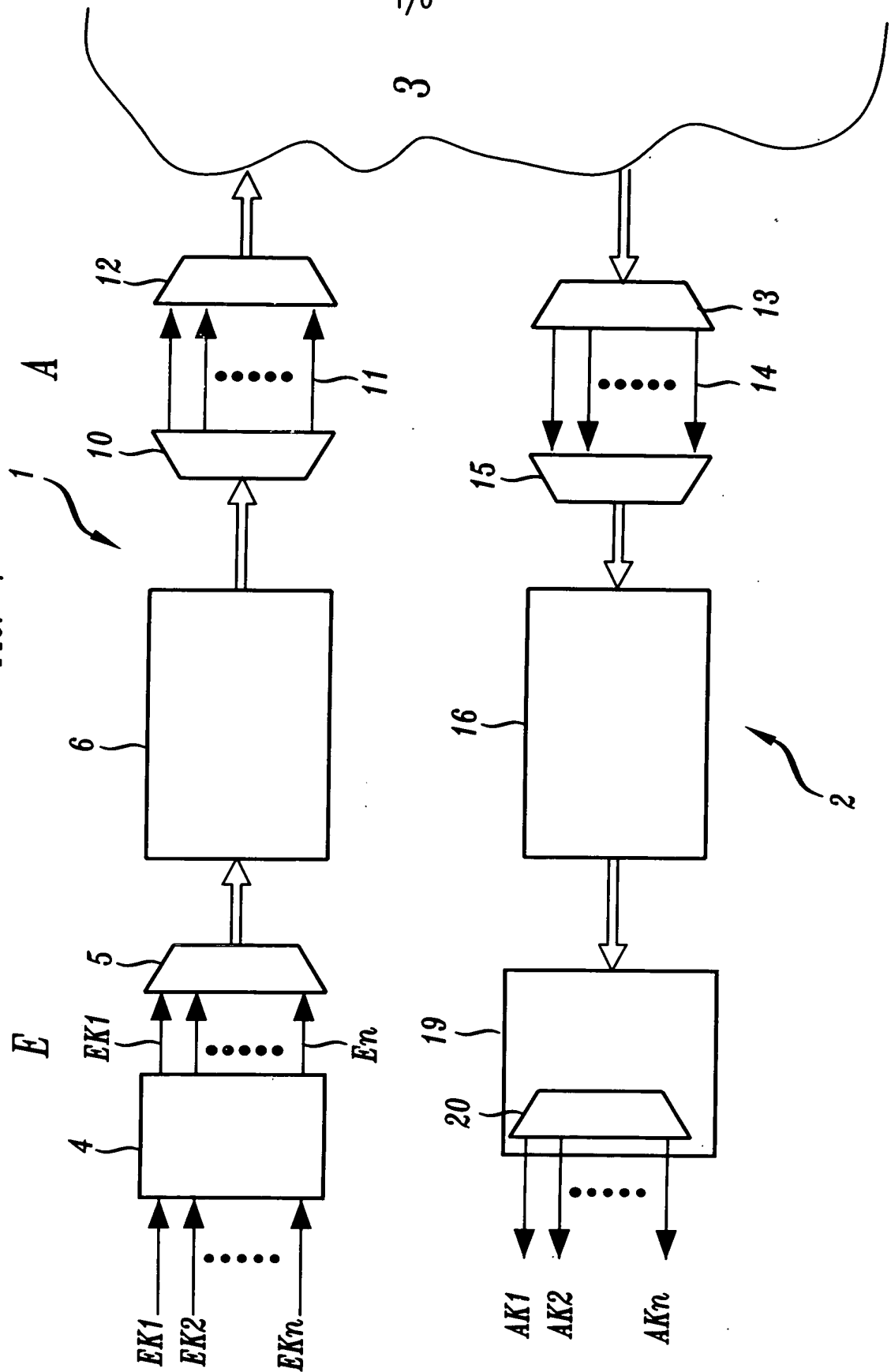


FIG. 2

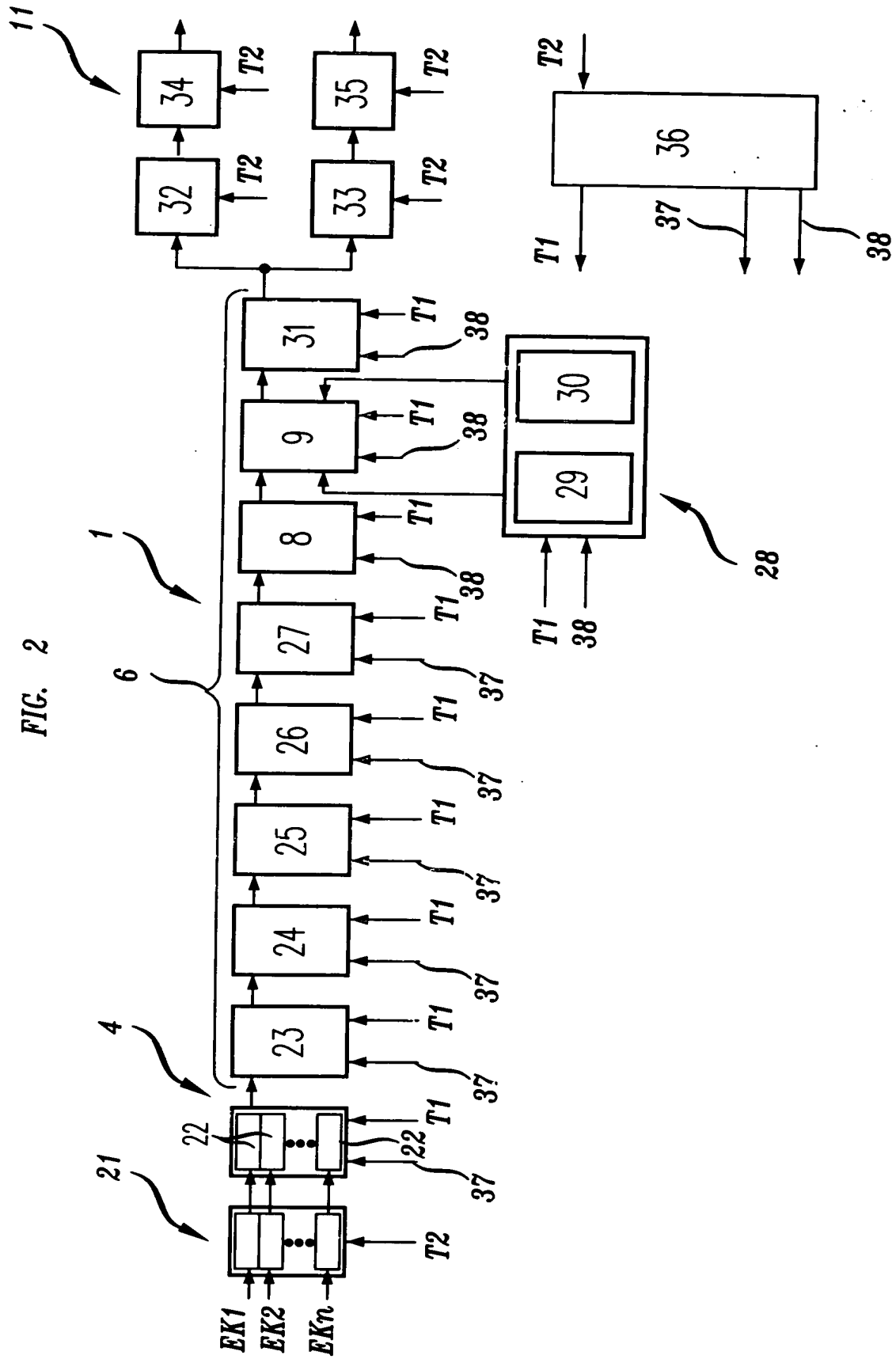


FIG. 3

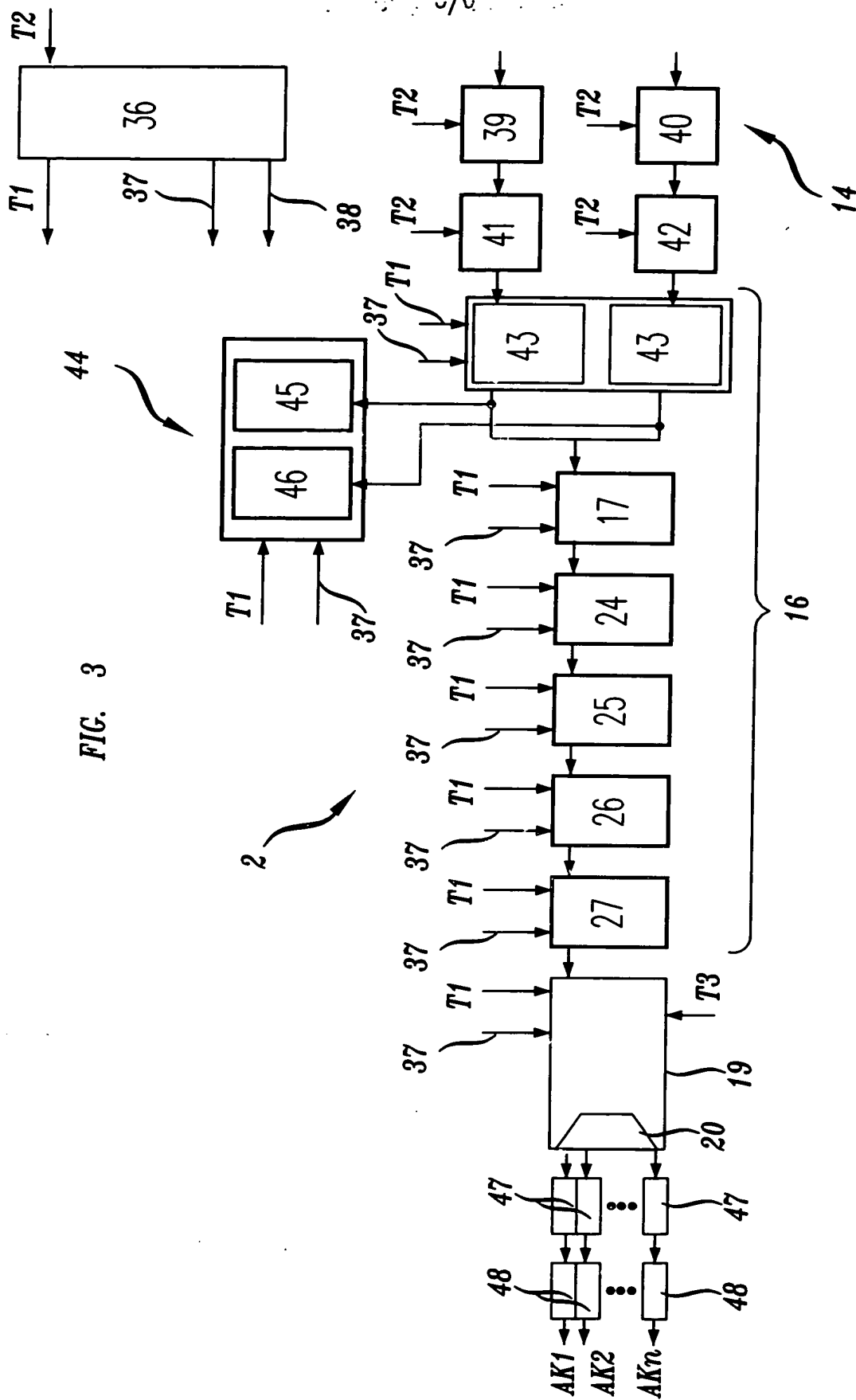
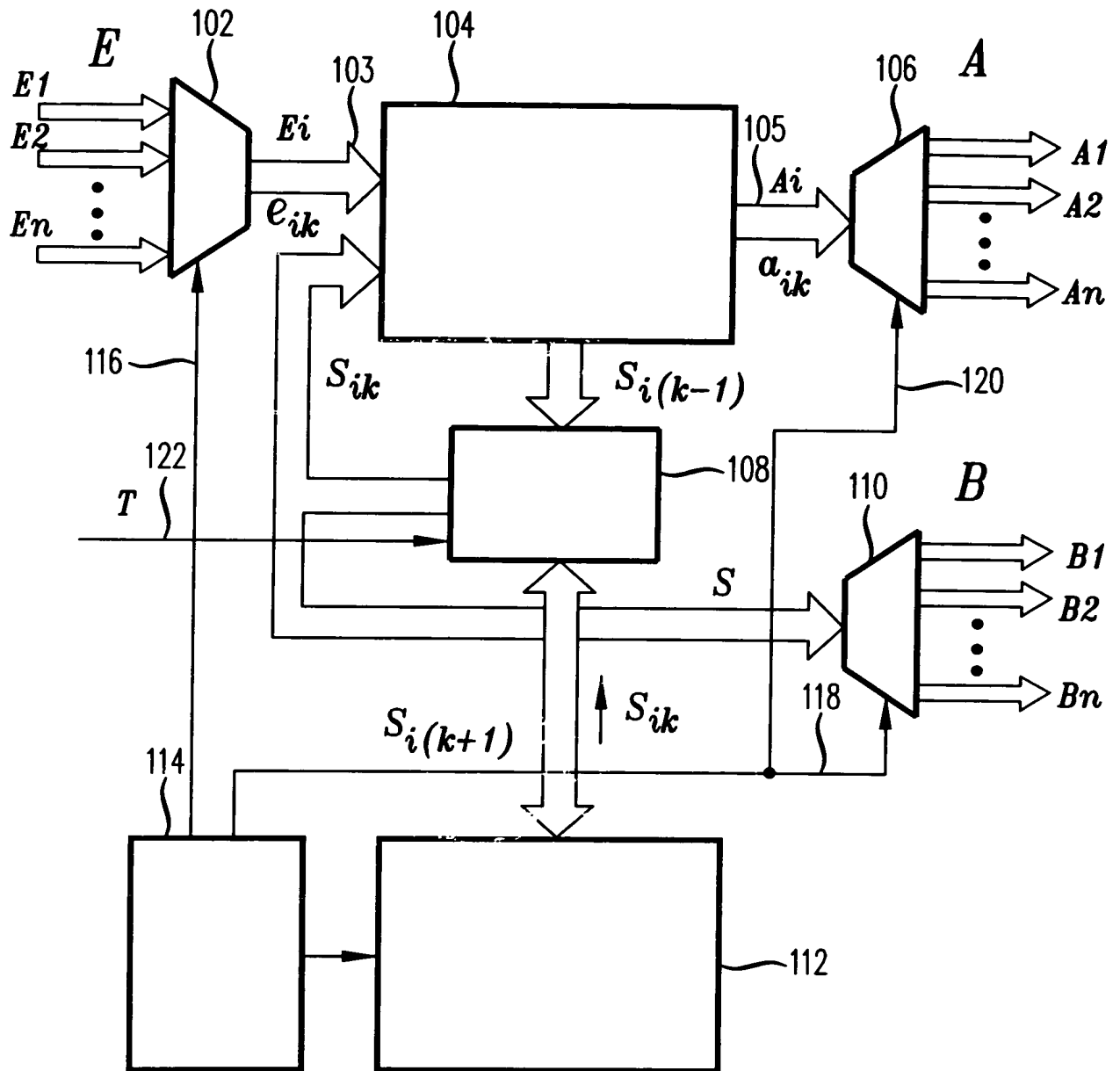


FIG. 4





Timing diagram for the 74164 8-bit shift register. The diagram shows eight clock signals (E1-E8) and five data signals (122 j T, 126 j i-1, 128 j W, 132 j i+1, 102 j i). The clock signals are periodic square waves. The data signals are shown as sequences of bits in a grid. The 122 j T signal is a high-frequency square wave. The 126 j i-1, 128 j W, 132 j i+1, and 102 j i signals are shown as sequences of bits in a grid, with the 102 j i signal being the most complex, showing a sequence of bits that changes over time.

122 j T

126 j i-1

128 j W

132  $j^{i+1}$

102 j*i*